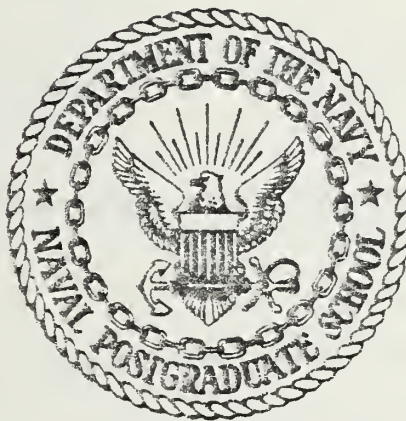DESIGN AND PERFORMANCE OF A FREQUENCY
HOPPING COMMUNICATIONS SYSTEM
USING DELTA MODULATION.

Habib Kucukoglu

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

DESIGN AND PERFORMANCE OF A
FREQUENCY HOPPING COMMUNICATIONS SYSTEM
USING DELTA MODULATION

by

Habib Kucukoglu

December 1978

Thesis Advisor: G. Myers

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

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Design and Performance of a
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by

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Lieutenant, Turkish Navy
B.S.E.E., Naval Postgraduate School, 1977

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requirements for the degree of

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hopping rate of 100 hops per second is used in the design.

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ACKNOWLEDGEMENT

I. INTRODUCTION

This study considers the performance of a frequency hopping (FH) voice communications system. With FH, the carrier frequency of the radiated signal is caused to vary in a discrete manner (hop) over some predetermined range. The hop rate is a variable in the design.

In a typical FH system, the analog voice signal is converted to a digital signal. The digits (bits in binary conversion) are then transmitted. The receiver converts the digital signal back to analog form. Pulse code modulation is a common form of analog-to-digital conversion (ADC). In this work, a new integrated circuit (IC) delta modulator was chosen for the ADC.

This report presents the design, characteristics, and test results of a particular frequency hopping system that uses delta modulation for ADC. The quality of the recovered signal is excellent for data rates as low as 25 kilobits per second. A hopping rate of 100 hops per second is used in this system.

II. BACKGROUND

A. FREQUENCY HOPPING

Frequency hopping (FH) is one possible type of spread spectrum system. FH can be defined as data transmission using many frequency channels in a predetermined sequence as shown in Fig. 1.
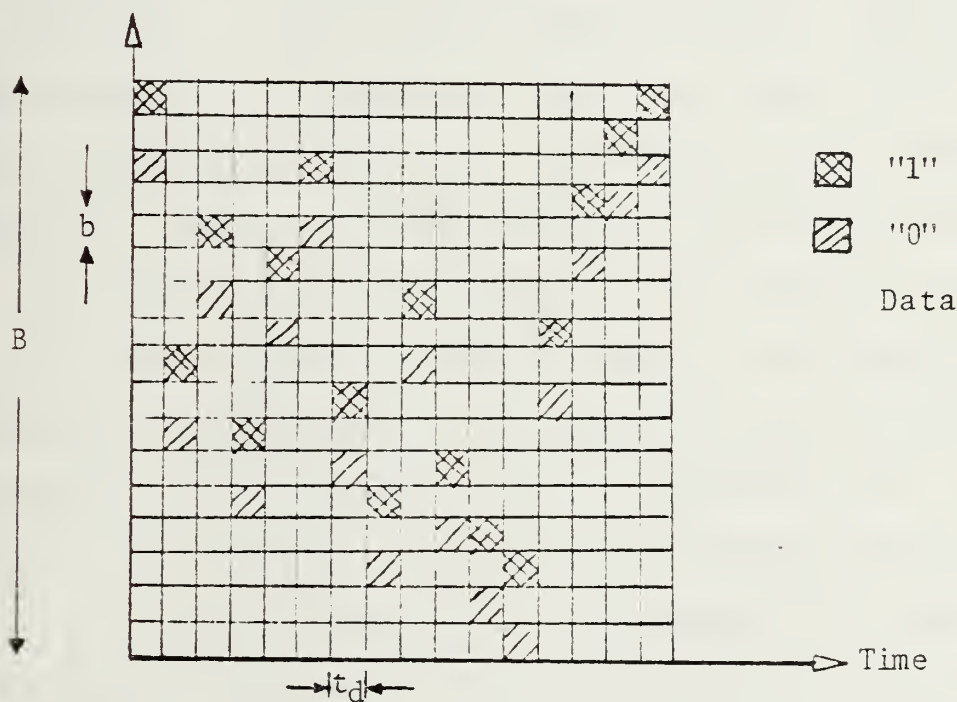

FIG. 1. FREQUENCY-TIME DIAGRAM OF A FH SYSTEM

In the figure shown above B is the total available bandwidth whereas b corresponds to the system bandwidth per hop. The dwell time in a particular frequency channel is given as t_d. Binary data can be sent by using frequency offset as shown in Fig. 1.

It can be readily shown that FH systems provide some immunity to jamming. A detailed discussion of FH system performance is given in Ref. 1. A simplified block diagram of a frequency hopping transmission system is given in Fig. 2.

For FH systems, high speed, digitally programmed frequency synthesizers are usually used. The pseudo random (PR) sequence generator of Fig. 2 provides a long repeating sequence of bits. The value of the output frequency of the synthesizer is selected by subgroups of this pseudo random sequence. Thus, the output frequency of the synthesizer "hops" to a new value whenever a different command comes from the binary pseudo random code generator. Then, the data modulates the hopped signal.

A simplified block diagram of a FH receiver is shown in Fig. 3. The receiver system contains a synchronized PR code generator and a frequency synthesizer which serves as a synchronous local oscillator. The IF amplifier has a bandwidth greater than b Hertz. A transmitted signal having frequencies: f_1, f_2, ...f_n is converted to a constant IF by means of the synchronous local oscillator in the receiver. Therefore, the bandwidth of the IF stage of a FH receiver is determined by the data bandwidth and the carrier modulation technique used.
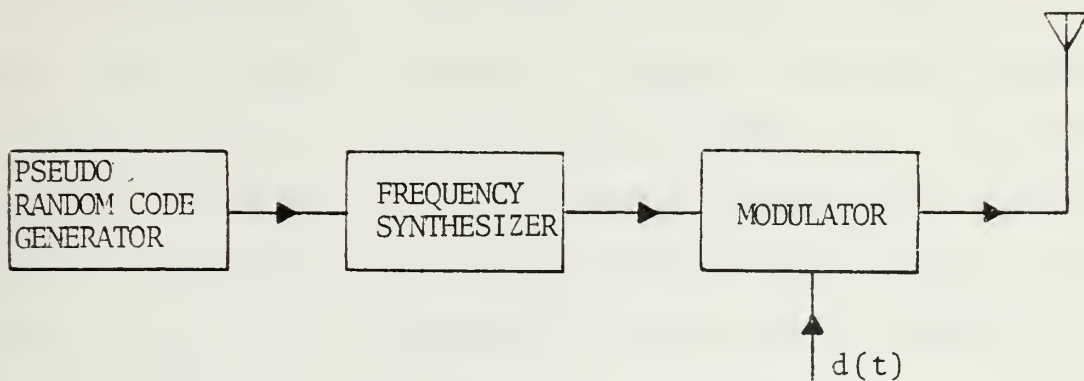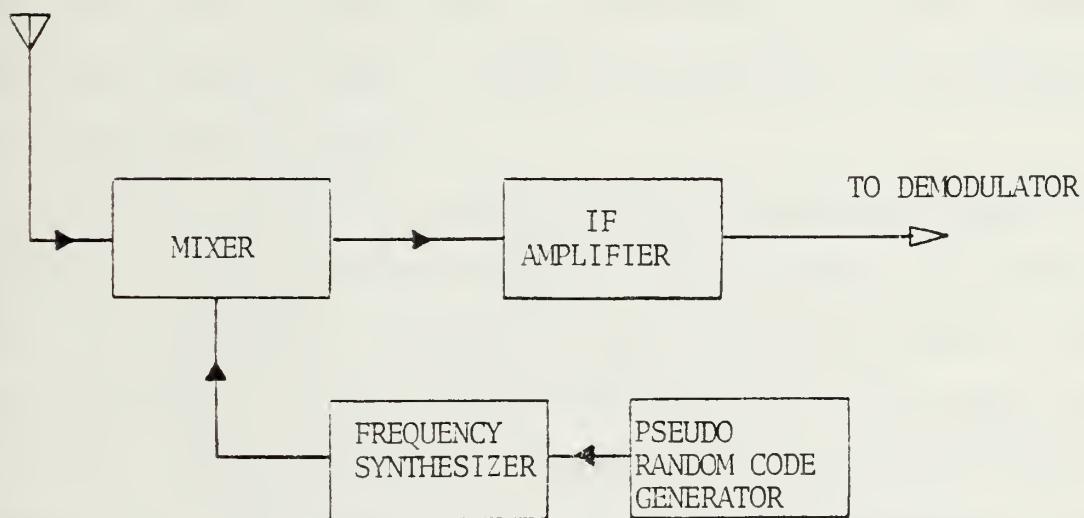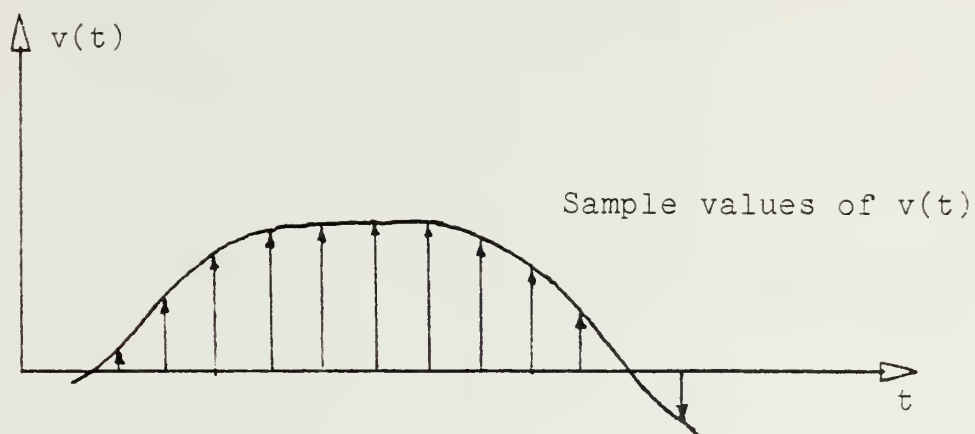
FIG. 2.   FREQUENCY HOPPING (FH) TRANSMITTER

FIG. 3.   A FH RECEIVING SYSTEM

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B. DELTA MODULATION

Delta modulation is one technique used to convert an analog message into a digital waveform. A basic difference between pulse code modulation (PCM) and delta modulation is that PCM represents the magnitude of the analog voltage while delta modulation represents the slope of the analog voltage as shown in Fig. 4. The block diagram of a basic delta modulator is given in Fig. 5.

The delta modulation technique of Fig. 5 is improved by using variable slope delta (VSD) and continuously variable slope delta (CVSD) modulation algorithms. The practical results obtained by using these algorithms are improved fidelity and wider dynamic range. The block diagram of a CVSD modulator is shown in Fig. 6.

For this project, a single chip CVSD modulator/demodulator is used to digitize the message. The bit rate is the same as the clock frequency. Using a 25 kHz clock rate gave a good performance for a voice signal bandlimited to the range 300 Hz to 3 kHz. The oscilloscope traces in Fig. 7 show the CVSD outputs for a sinusoidal input at different frequencies and different sampling rates.

a) Analog Voltage

b) Output of Delta Modulator

c) Discrete From of v(t) = $\int$ d(t) dt

FIG. 4. BASIC DELTA MODULATION WAVEFORMS

FIG. 5. BASIC DELTA MODULATION

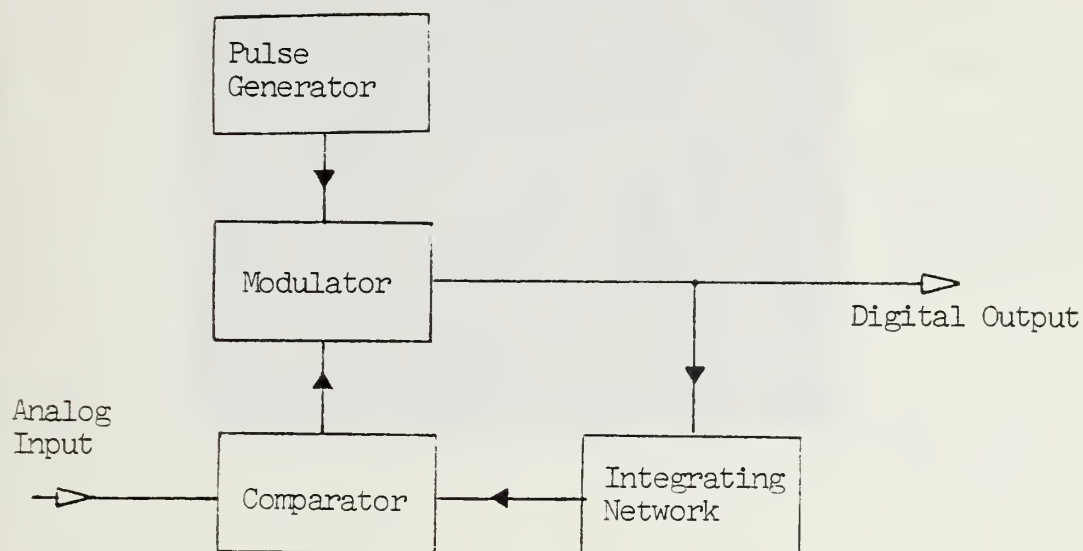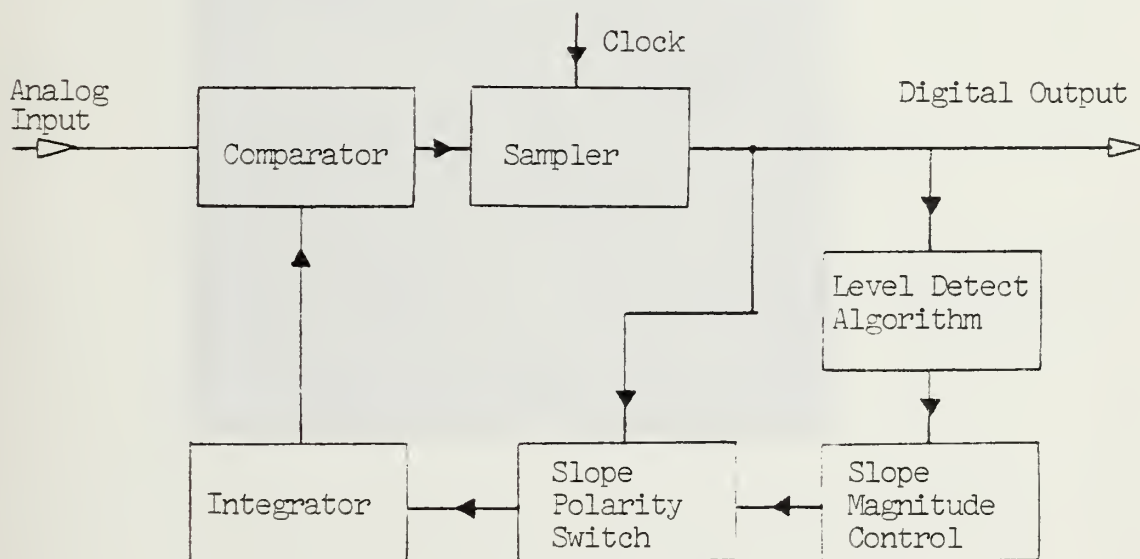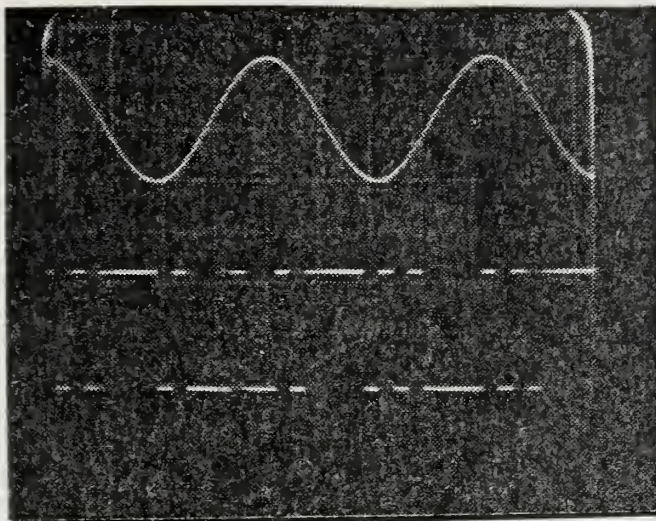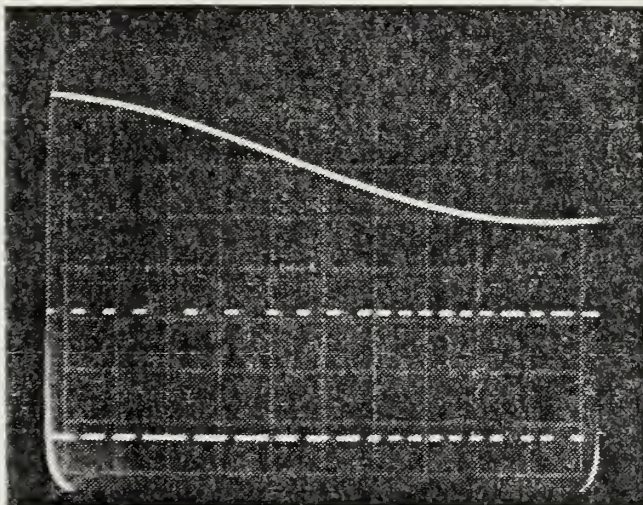

FIG. 6. CVSD MODULATOR BLOCK DIAGRAM

a) f_{sig} = 1.2 kHz

b) Delta Modulator
output at
25 kbit/sec

a) f_{sig} = 100 Hz

b) Delta Modulator
output at
10 kbit/sec

FIG. 7.   CVSD MODULATOR

The delta demodulator is basically an integrator. How-
ever, the CVSD demodulator contains additional circuitry
similar to that in the modulator. A block diagram of the
CVSD demodulator is shown in Fig. 8.

```
                         ↓ Clock
  Digital
  Input    ┌──────────┐         ┌──────────┐      ┌──────────┐
    ──────→│          │      ┌─→│ Level    │      │ Slope    │
           │ Sampler  │──────┤  │ Detect   │─────→│ Magnitude│
           │          │      │  │ Algorithm│      │ Control  │
           └──────────┘      │  └──────────┘      └──────────┘
                             ↓                          │
                             │                          │
  Audio                      ↓                          │
  Output   ┌──────────┐  ┌──────────┐                   │
    ←──────│Integrator│←─│ Slope    │←──────────────────┘
           │          │  │ Polarity │
           └──────────┘  │ Switch   │
                         └──────────┘
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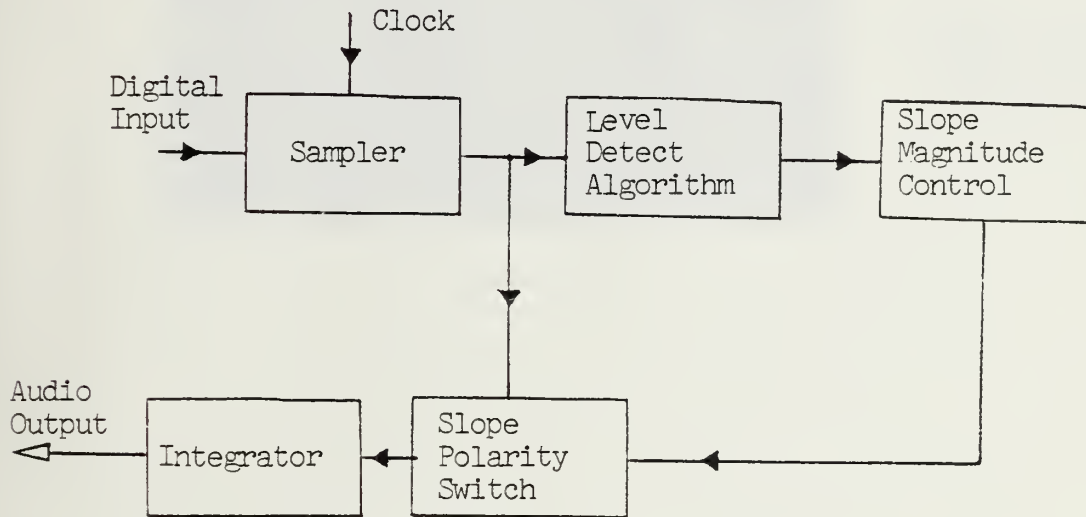
FIG. 8.   CVSD DEMODULATOR BLOCK DIAGRAM
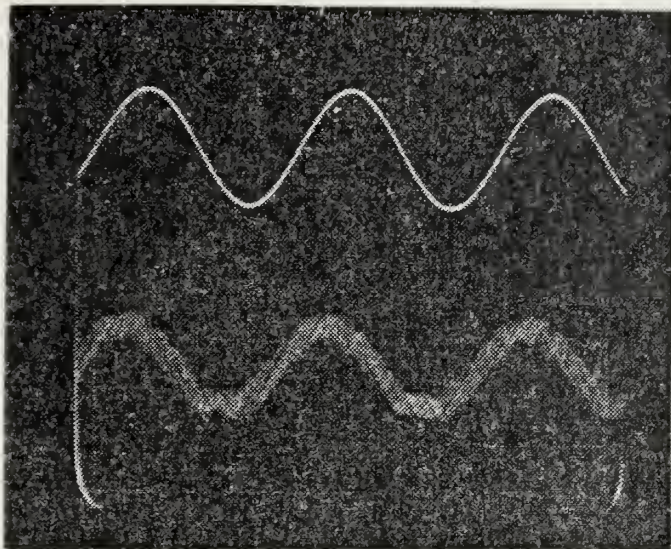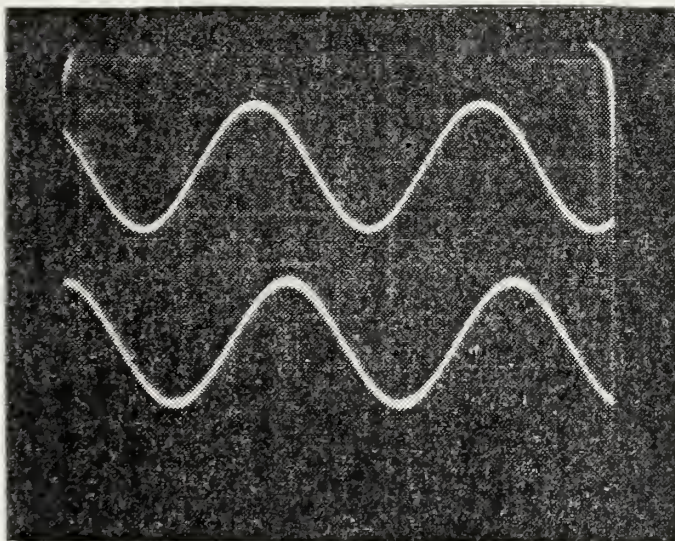

The oscilloscope traces of the sinusoidal inputs to the
modulator and the reconstructed sinusoidal waveforms at the
output of the CVSD demodulator are shown in Fig. 9.

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a) Original analog
signal
(f = 1.1 kHz)

b) CVSD demodulator
output before
low-pass filtering

a) Original analog
signal
(f = 1.1 kHz)

b) CVSD demodulator
output (after
low-pass
filtering

FIG. 9.   CVSD DEMODULATOR

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III. THE EXPERIMENTAL SYSTEM

The block diagram of the experimental frequency hopping transmitting-receiving system is shown in Fig. 10. For this application, voice is used as the message. The analog signal, v(t), is digitized by a delta modulator. The two-level (bipolar) voltage frequency modulates a carrier whose frequency is caused to hope in a pseudo random manner.

The receiver de-hops the transmitted signal with a synchronously hopping local oscillator. Thus, the receiver IF remains constant. In this work, no attempt was made to isolate the receiver and transmitter. Receiver synchronization was provided by hardwire from the transmitter section. A frequency demodulator extracts the digitized message. This signal is converted to the analog equivalent, v(t) by a delta demodulator. The audio is filtered and amplified by the final stages and applied to a speaker.

A single clock with frequency dividing circuitry provides the adequate hopping rate and analog data sampling rate for delta modulation/demodulation. The building blocks of the system are described in the following sections.
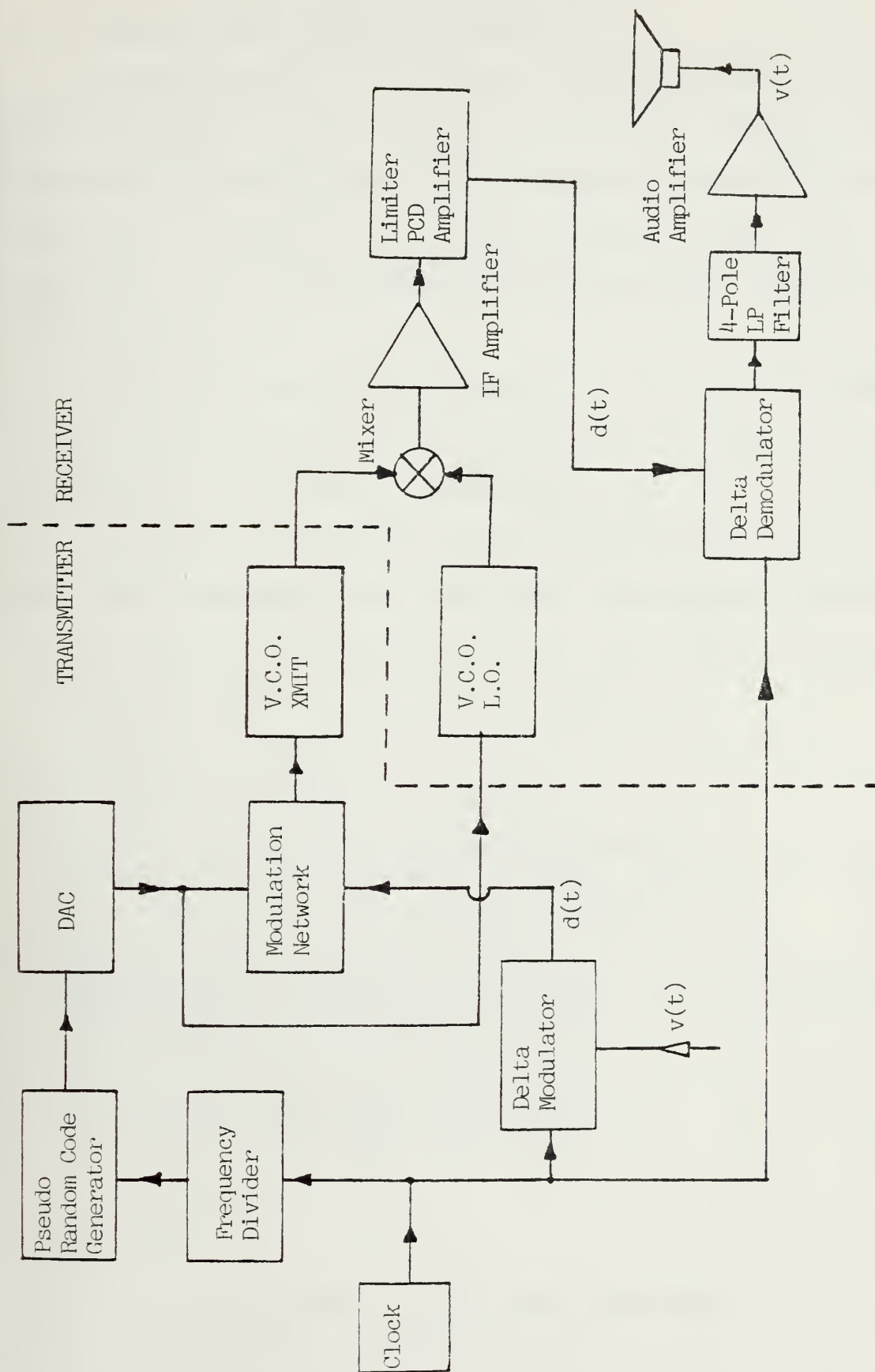
FIG. 10. BLOCK DIAGRAM OF THE FREQUENCY HOPPING TRANSMITTER-RECEIVER

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A. PSEUDO-RANDOM SEQUENCE GENERATOR

A pseudo-random (PR) sequence code generator is an essential part of many spread spectrum (SS) systems. In a frequency hopping system, these codes can be used to determine the hopping pattern of the RF signal. These codes are generated with maximal length code generators (feedback shift registers).

For this project, six stages of an 8 bit shift register (74164) and an EX-OR gate (7486), which is modified as an EX-NOR gate, are used for generating a $2^6 - 1 = 63$ bit length code by making the feedback connections shown in Fig. 11. The shift register states and their corresponding decimal values are listed in Table 1. The output voltage (sequence) of the code generator is shown in Fig. 12.
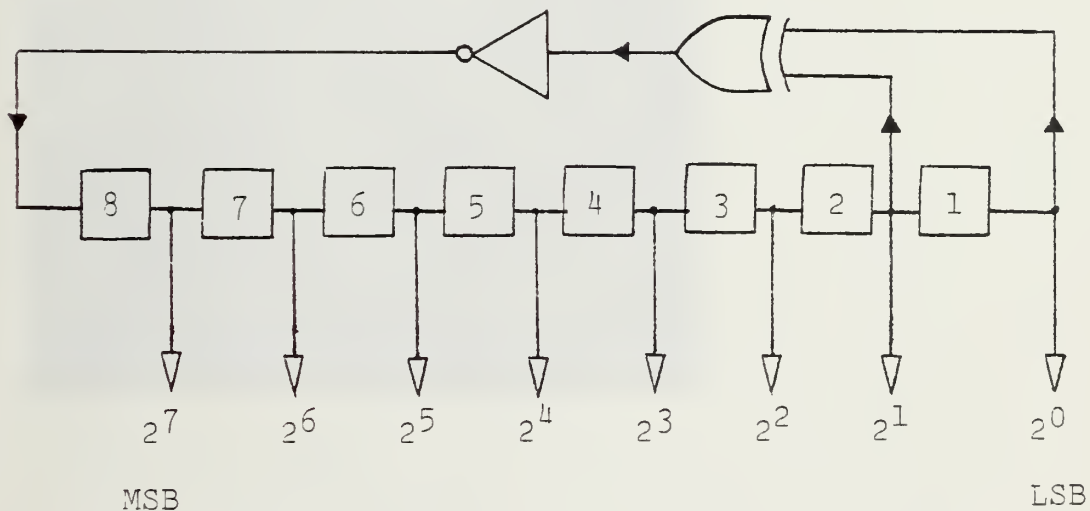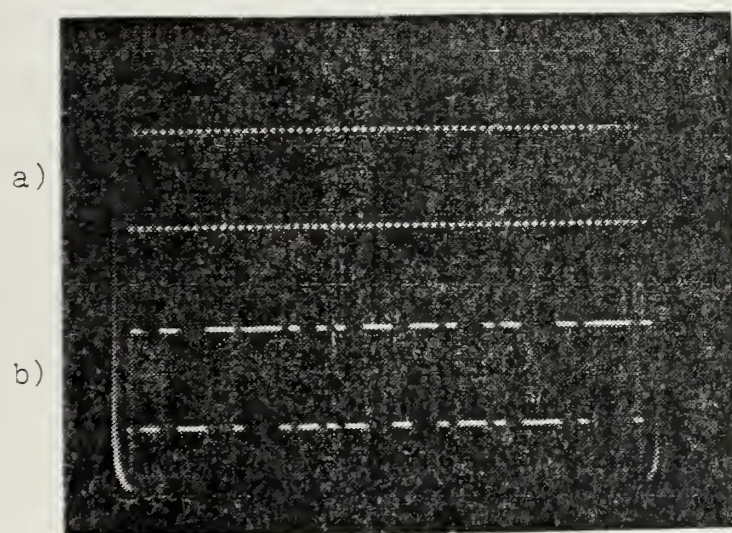

FIG. 11.   PSEUDO RANDOM CODE GENERATION

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Clock Pulse	Decimal Number	Clock Pulse	Decimal Number	Clock Pulse	Decimal Number	Clock Pulse	Decimal Number	Clock Pulse	Decimal Number	Clock Pulse	Decimal Number	Clock Pulse	Decimal Number	Clock Pulse	Decimal Number
1	0	9	127	17	63	25	95	33	15	41	119	49	51	57	85
2	128	10	191	18	159	26	175	34	135	42	187	50	153	58	42
3	192	11	223	19	207	27	215	35	195	43	221	51	76	59	21
4	224	12	239	20	231	28	235	36	225	44	110	52	166	60	10
5	240	13	247	21	243	29	245	37	112	45	55	53	83	61	5
6	248	14	251	22	249	30	122	38	184	46	155	54	169	62	2
7	252	15	253	23	124	31	61	39	220	47	205	55	84	63	1
8	254	16	126	24	190	32	30	40	238	48	102	56	170	64	0

TABLE 1.   DECIMAL EQUIVALENT OF THE PR SEQUENCE

a) Clock input
b) PR code sequence

FIG. 12.   PR CODE GENERATION

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A frequency divider and reset circuit are part of the code generator as shown in Fig.13 . The frequency divider determines the hopping rate. It is capable of dividing the clock frequency by 1, 2, 4 ... 256 by suitable programming. The schematic diagram of the frequency divider is given in Appendix.

For EX-NOR operation, all "ones" in the shift register will cause the sequence to stop. This does not occur theoretically since the contents of the shift register is all "zeros" when the voltage is applied to the system. However, transients and different delay times may cause the contents to be all "ones" at some time. A way to prevent the all ones state from persisting is to use an 8 - Input NAND gate which generates a "0" whenever all ones appear. This "0" clears the contents of the shift register and starts the sequence again.
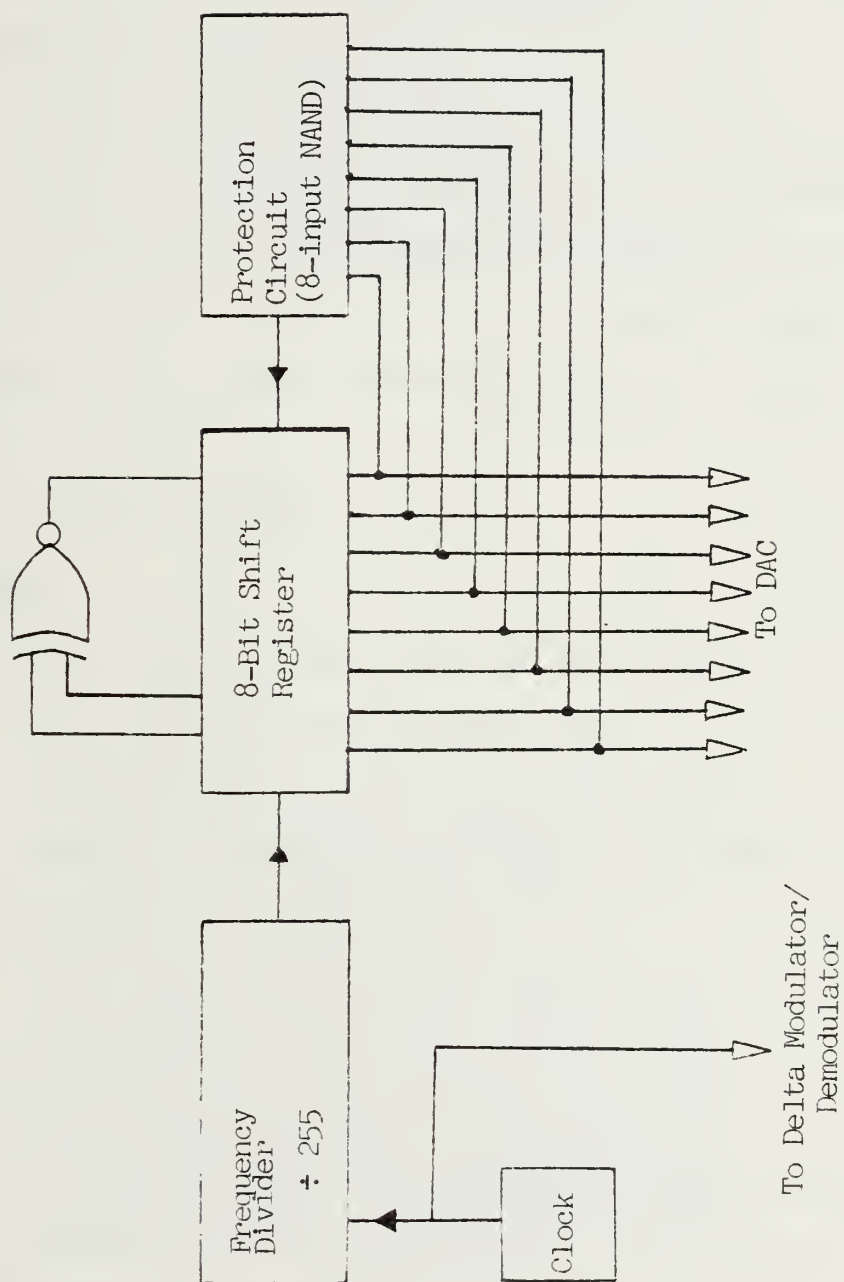
FIG. 13. PR CODE GENERATOR WITH PROTECTION CIRCUIT

B. DIGITAL TO ANALOG CONVERTER (DAC)

To use the code generator output for frequency hopping, the decimal equivalents of the binary codes must be obtained. Discrete voltage levels, which are used to "hop" the frequency of an oscillator, are generated from the PR sequence (or codes) by means of a DAC.

For this application, an 8-bit, high speed DAC (DAC-08 BC) followed by an op-amp (μ741) worked well. The decimal values listed in Table 1 are converted to voltage levels such that decimal "0" gives 0 volt output and decimal "255" gives 10V. The output stage of the DAC can be given for any state as follows

$$V_o(nT) = \frac{10}{255} D$$

where

D is the decimal value in that state
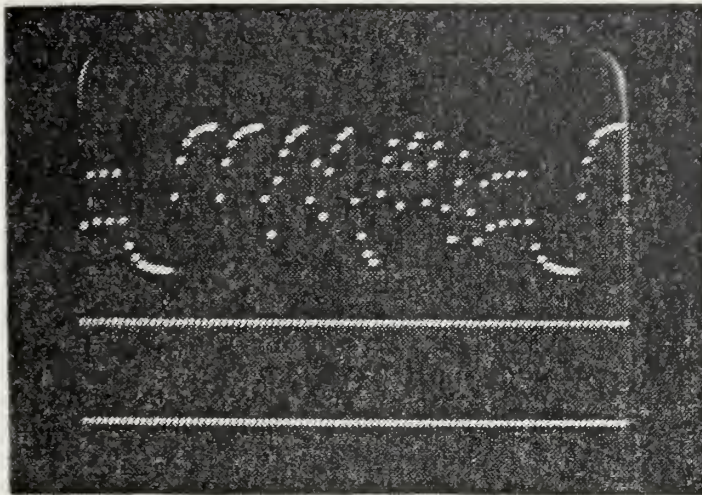
T is the duration of that state

$0 \leq n \leq 63$

For example, the output voltage of the DAC at state 30 is (from Table 1),

$$V_o = \frac{10}{255} \cdot 122 = 4.78 \text{ Volts}$$

These voltage levels are shown in Fig. 14.

In Fig. 14b, the level transition times are a few microseconds (because of the op-amp used). This limits the rate of frequency hopping. In this application the data rates of 25 KBits/sec and hopping rates of 100 hops/sec were easily compatible with the microsecond transition times.

a) 63 bit period
of DAC output
voltage

b) Clock
f = 25 kHz

FIG. 14a.   PR SEQUENCE

a) Discrete voltage
levels of DAC
output

b) Clock
f = 25 kHz

FIG. 14b.   PR VOLTAGE LEVELS

C. MODULATION NETWORK

The message $v(t)$ is converted to a digital waveform $d(t)$ by using delta modulation, and $d(t)$ then modulates a carrier. For this application, FM (or frequency shift keying, FSK, for digital FM transmission) is used.

The modulation network combines the hopping voltage and modulation voltage. Thus, the output of the modulation network is

$$V_m \text{ out} = k_1 V_{hop} + k_2 d(t)$$

where the constants k_1 and k_2 are chosen to give the desired performance. The block diagram of the modulation network is given in Fig. 15. The data modulator provides the data modulation without interfering with the receiver VCO.

The output voltage waveform of the data modulator is shown on the oscilloscope trace of Fig. 16.

D. VOLTAGE CONTROLLED OSCILLATOR

An essential part of a frequency hopping system is the voltage controlled oscillator. Some of the key parameters of a VCO are: frequency stability, frequency range, linearity, and response time.

For this application, two VCOs are used. One for the transmitter and one as a receiver local oscillator. Both are built from TTL NOR gates connected to form a multivibrator. The shematic diagram is shown in the Appendix.

DAC output

$V_h(t)$

k_1

$k_1V_n(t)$

$+$

Σ

to VCO (XMTR)

$k_1V_n(t)$
$+ k_2d(t)$

$-$

$-k_2d(t)$

k_3

$-k_2$

d(t), data signal
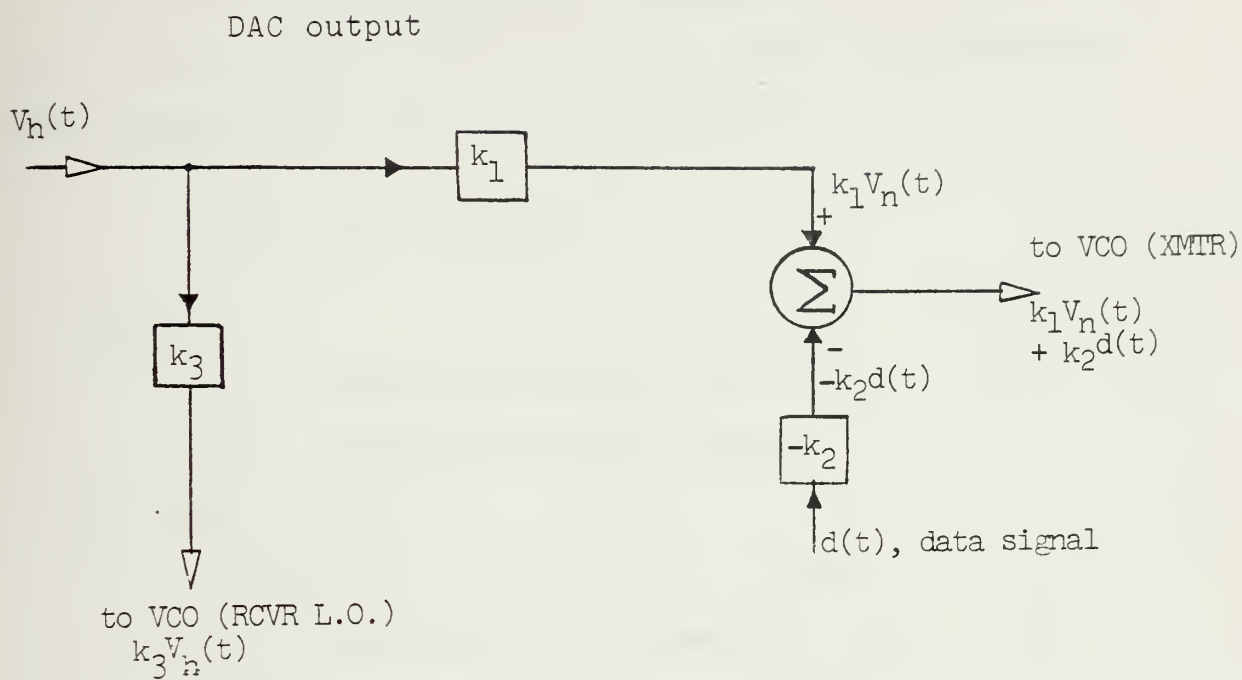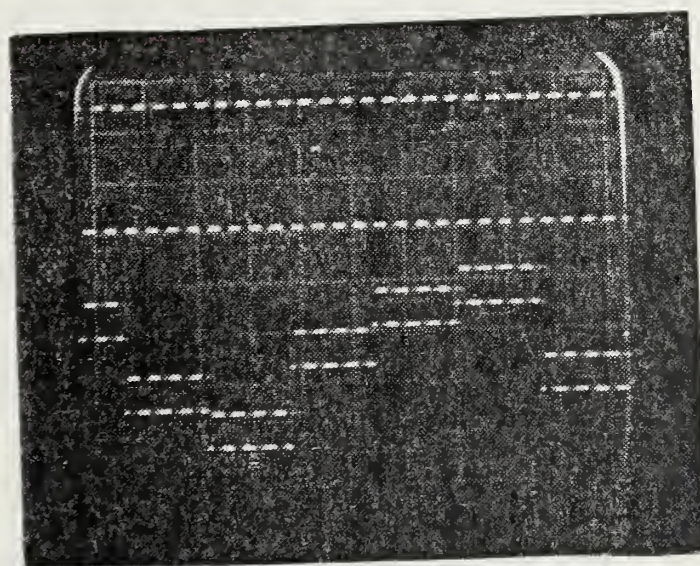
to VCO (RCVR L.O.)
$k_3V_n(t)$

FIG. 15.   MODULATION NETWORK BLOCK DIAGRAM

a) Data input

b) Output of data
   modulation
   network

FIG. 16.   MODULATION NETWORK OUTPUT

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When the output of the DAC is applied to the input of a VCO, the frequency of the RF signal "hops" to a new value. The frequency of a VCO can be formulated as

$$f(V_c) = f_o + \frac{V_c}{V_{c\ max}} \Delta f$$

where

V_c = control voltage of VCO

Δf = Maximum frequency change

For this project

$V_{c\ max}$ = : 5.0V and Δf = 656 kHz

f_o = 1024 kHz for transmitter VCO

f_o = 1690 kHz for reciever VCO.

The frequency versus voltage curves of the VCOs are shown in Fig. 17.

Linearity of the VCO is very good in the ranges shown in Fig.17. For FSK modulation this property is not very important since only two different frequencies are used. However, in FH the number of channels used are large. These frequency channels must be equispaced depending on the RF modulation technique used.

E. MIXER

The receiving system utilizes a double balanced mixer (RELCOM-MI) which provides 50 dB rejection of the RF and local oscillator signals at the output.
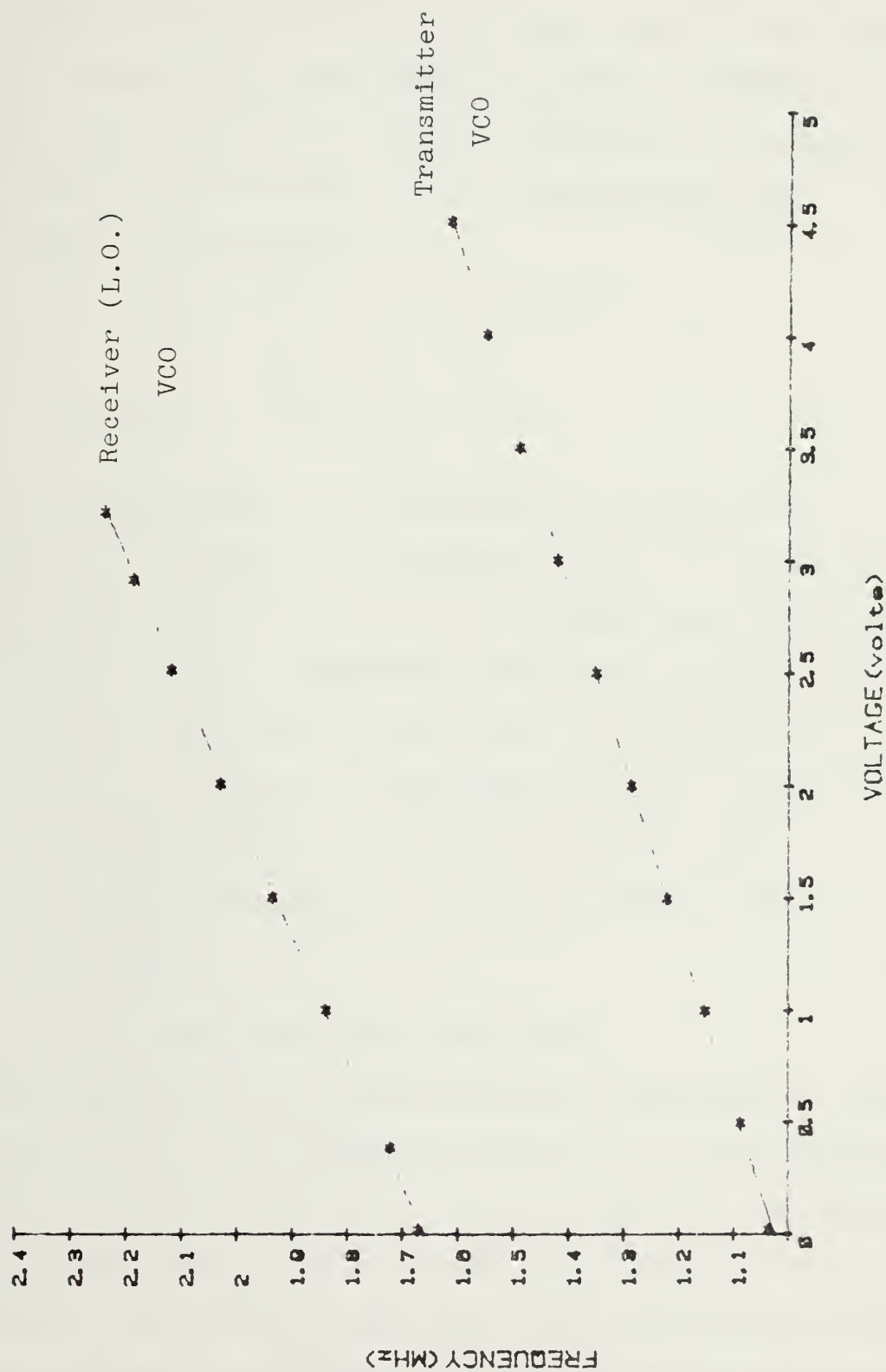
FIG. 17. VOLTAGE-FREQUENCY CHARACTERISTICS OF VCOS

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F. IF AMPLIFIER

With the mixer used, a conventional one-stage IF amplifier delivers adequate band selectivity and power gain for the data demodulation process. The IF amplifier circuit diagram with mixer stage is given in Appendix A-5. A high gain transistor (2N3404) is employed with input and output IF transformers. This amplifier has the following characteristics:

$$A_V = 1.2$$
$$f_c = 645 \text{ kHz}$$
$$Bw \text{ (3dB)} = 68 \text{ kHz}$$

The voltage gain, A_V is measured at the secondary winding of the output IF transformer which is used for the low impedance interface of the next stage (amplifier/limiter transistor). The low impedance output with modest voltage gain provides considerable power gain. The bandwidth of this stage is adjusted to accommodate the FSK signal at a rate of 25 kilobits/sec. The result is also useful at 50 kilobits/sec (due to the limiting process of the following stage).

G. LIMITER, DEMODULATOR, DATA AMPLIFIER

The demodulator is a pulse counting discriminator. The relatively low center frequency (645 kHz) of the IF amplifier, the wide pass band (70 kHz) of the IF amplifier, the digital nature of the demodulated waveform, and the simplicity of the design and operation make this type of demodulator more attractive than others (ratio detectors or phase-locked loops).

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H. PULSE COUNTING DEMODULATOR (PCD)

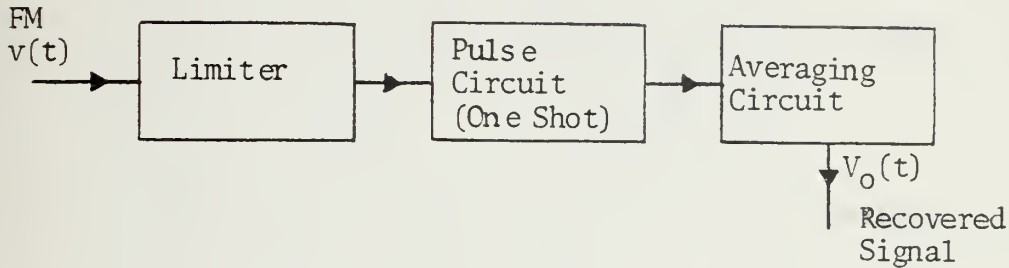The block diagram of a PCD is shown in Fig. 18.

FIG. 18. PULSE COUNTING DISCRIMINATOR

The operation of PCD is illustrated in Fig. 19. When an unmodulated RF signal is applied to the system, the limiting action shapes the waveform as shown in Fig. 19a. The limiter output is rectified by a half wave rectifier and applied to the monostable multivibrator (one shot). It generates pulses $V_a(t)$ of constant duration $= \tau$ sec. The average of these pulses has a constant DC value $V_o(t)$. However, any FM signal has a non-constant time T for one cycle of the carrier. The inverse of T is proportional to the message amplitude. These variations cause the DC level of the output $V_o(t)$ to change at the same rate as the modulating signal waveform. In this manner, a replica of the message is obtained as $V_o(t)$.

For this application, the output of the monostable multi-vibrator (74121) is averaged by a two-stage RC low-pass filter. The demodulated data waveform is amplified in the first stage of the amplifier. Before the next stage, another low-pass filter is used to decrease the high frequency content of the final amplifier-limiter output. The output is TTL compatible.

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(a) V(t) Unmodulated Signal

(b) $V_c(t)$ Limiter

(c) $V_a(t)$ A constant DC level V_o

(d) FM Signal
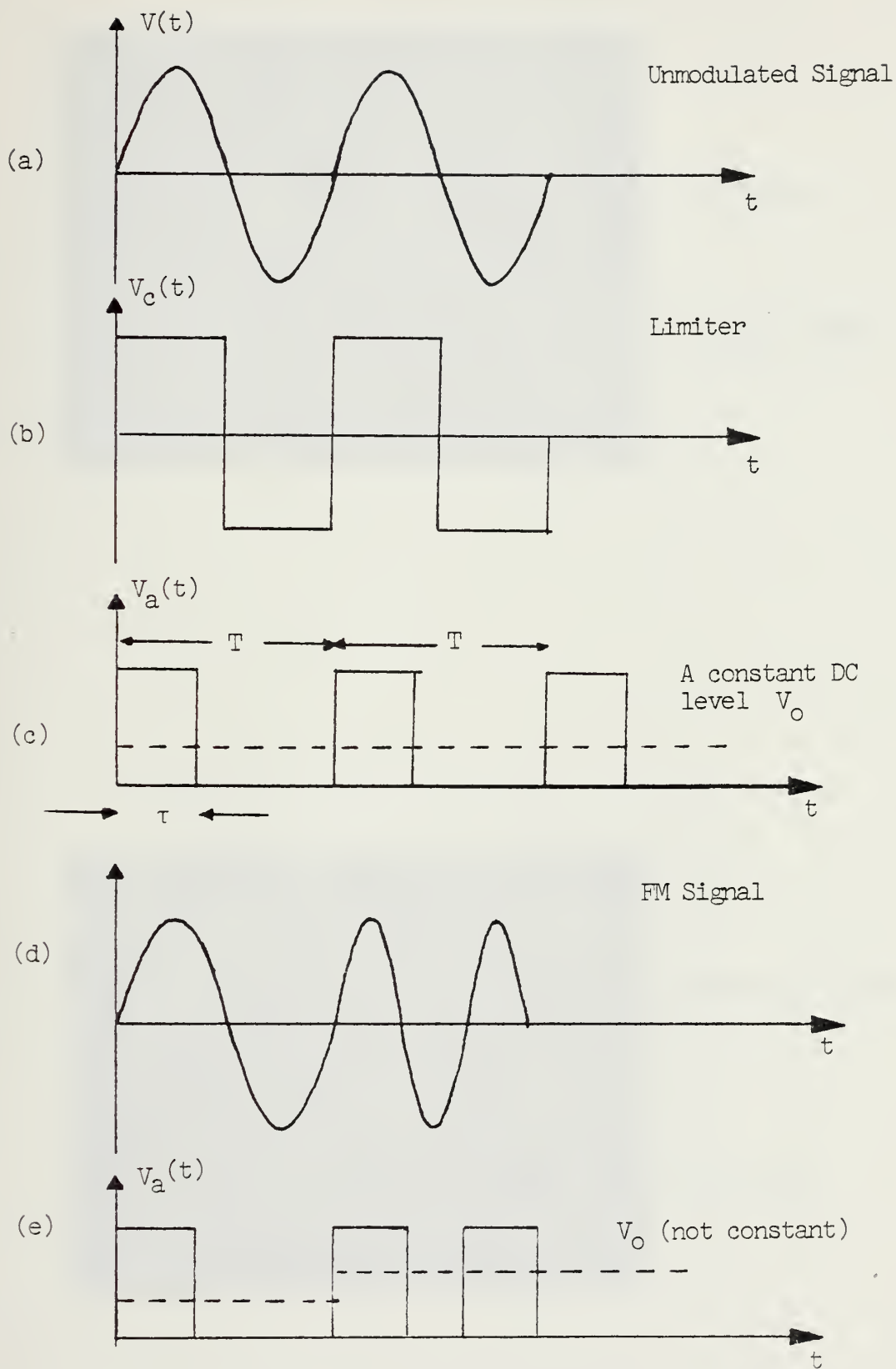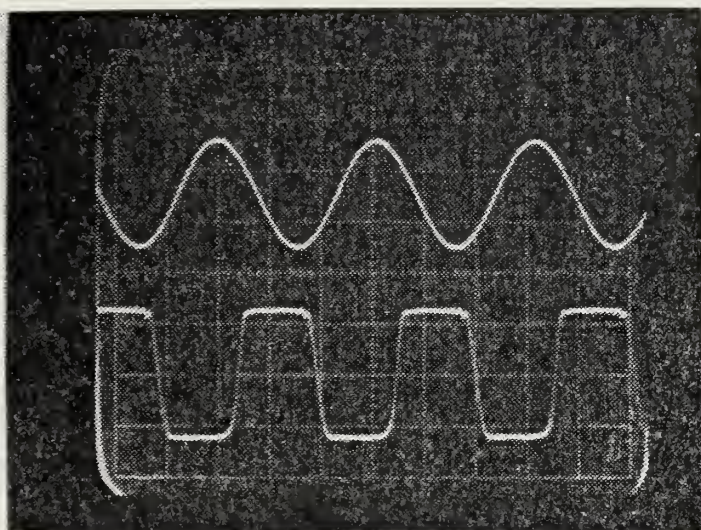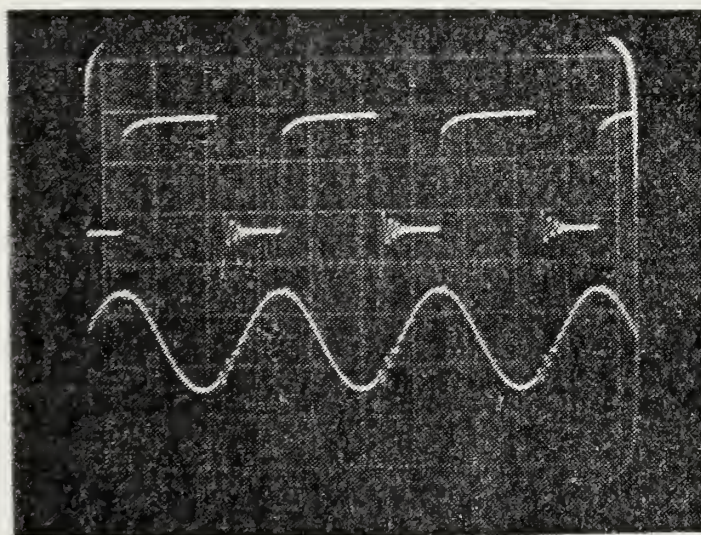
(e) $V_a(t)$ V_o (not constant)

FIG. 19. PCD OPERATION

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a) IF input

b) Limiter output

a) One-shot output

b) IF signal

FIG. 20.   PCD

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The schematic diagram of the PCD is given in Appendix A-8 .
Limiter action and pulse generation are shown in Fig. 20.

I. AUDIO AMPLIFIER

The output of the CVSD demodulator reconstructs the analog
message, $v(t)$. However, a one stage low pass filter employed
for this purpose is not adequate. The level of the high fre-
quency components shown in Fig. 9a must be reduced. For this
reason a four-pole active Butterworth lowpass filter is used
to recover the original message, $v(t)$. Its cut-off frequency
is chosen as 3.1 kHz. The result is shown in Fig. 9b. To
provide audio power level required to drive a speaker, an IC
audio amplifier (LM 380) is used.

CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

A frequency hopping system is one choice available for military communication systems. Jamming resistance is the major advantage in the military allocated RF spectrum. The system designed and built as part of this project worked well. The results of overall data modulation-demodulation process including frequency hopping and dehopping are shown on the osciloscope traces in Fig. 21.
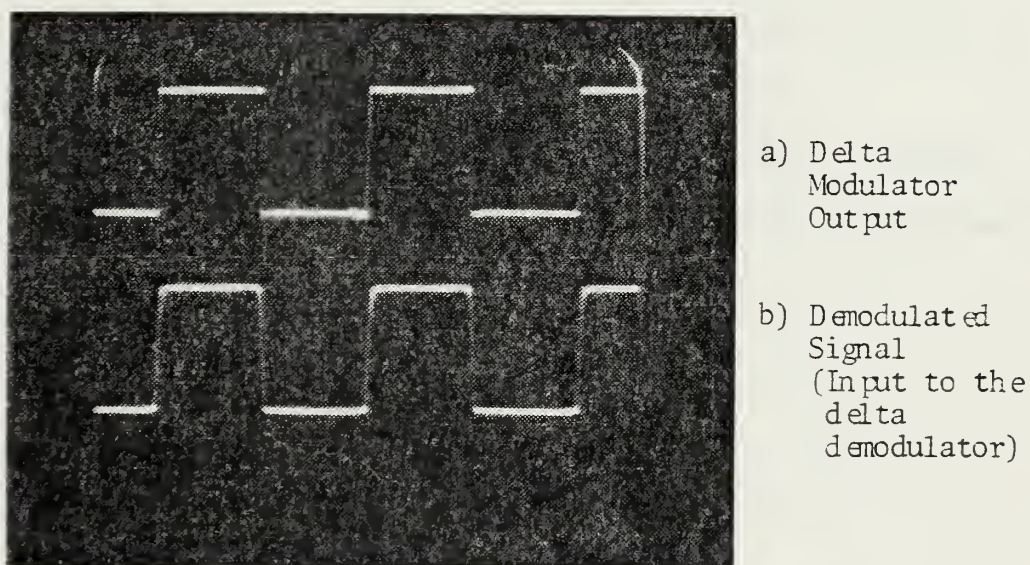

a) Delta
   Modulator
   Output

b) Demodulated
   Signal
   (Input to the
   delta
   demodulator)

FIG. 21. FREQUENCY HOPPING SYSTEM PERFORMANCE

B. RECOMMENDATIONS

To improve the jamming immunity of FH systems, the number of frequency channels possible should be large. A higher frequency VCO with better stability could also give improved results. Alternatively, a high speed frequency synthesizer with two outputs (one for the transmitter section and the other for the receiver L.O. injection) can completely eliminate the mismatching problem between the transmitter and receiver.

For digitization of the voice signal, delta modulation seems to give good results with relatively low bit rates. The delta modulator-demodulator chip used for this worked well. Employing an additional low-pass filter section at the analog input of the delta modulator and providing additional low pass filtering at the output of the delta demodulator will give a higher signal-to-noise ratio for the voice signal.

A phase-locked loop can be employed as a carrier demodulator, if the center frequency of the IF amplifier is increased by using higher frequencies for transmission.

This appendix contains the schematic diagrams of all the circuits used in this work. The components used to implement the various systems include TTL gates (EX-OR, NAND, NOR gates), astable and monostable multivibrators, shift registers, counters, DAC, operational amplifiers, IC audio amplifier, and a single chip delta modulator/demodulator. Operating characteristics of each component are found in reference   .

The various circuit diagrams are presented in Figures A-1 through A-9 in the following order:

Fig A-1:   Clock and Frequency Divider

Fig A-2:   PR Code Generator with Protection Circuit

Fig A-3:   DAC

Fig A-4:   Carrier Modulator-Hopping Circuit

Fig A-5:   VCO

Fig A-6:   Delta Modulator/Demodulator

Fig A-7:   Mixer - IF Amplifier

Fig A-8:   Limiter - PCD Amplifier

Fig A-9:   LP Filter - Audio Amplifier

The values of all capacitors are in micro (10^{-6}) farads unless otherwise indicated.

Fig A-1 shows the clock and the divide by 255 counter.

The clock frequency was set at 25 kHz by choosing the
resistor and capacitor values indicated. The output of the
clock is directly applied to the delta modulator and demod-
ulator to first digitize the message and then reconstruct the
message from the digitized form respectively. The clock out-
put is also applied to the frequency divider. The output fre-
quency ($\frac{25,000}{255} \cong 100$ Hz) if the divider is applied to the PR
code generator.

In Fig A-2, an 8-Bit shift register (74164) with EX-OR
gates, one of which is used as an inverter, generates the 63
bit PR sequence by means of serial feedback. This shift regis-
ter is a serial in, parallel out type. This allows the outputs
to be applied to the DAC. An 8-Input NAND gate is also driven
from these terminals. Whenever all the contents (outputs) of
the shift register are "1", the NAND gate generates a "0" which
clears the shift register contents, thus starting the PR se-
quence again.

Fig A-3 is the schematic of the DAC. The decimal equiva-
lent of the digital input is first converted into a current
value. Then, this current (2 mA for decimal 255) is applied
to an external op-amp which converts this current to a voltage
(10 volts for decimal 255). The scale adjustment is made by a
potentiometer and zener diode.

The carrier modulator - hopping circuit shown in Fig A-4
has two op-amps (μ 741) and potentiometers. The first op-amp
isolates the data modulation input from the local oscillator
VCO hopping circuit. The final op-amp is used as a differential

amplifier which gives an output, $V_o = \dfrac{R_2}{R_1} (V_1 - V_2)$ where V_1 is the data output and V_2 is the hopping voltage. The output of the final op-amp is applied to the transmitter VCO. One of the potentiometers is used to match the local oscillator VCO of the reciver and the other one is used to set the frequency deviation of FSK for carrier modulation.

The VCO design in Fig A-5 uses a single package TTL quad 2-Input NOR gates (7402), two switching diodes, resistors, timing capacitors and a buffer stage. The capacitors C_1 and C_2 determine the operating frequency whereas R_1 and R_2 are used to adjust the frequency range of the VCO. The buffer stage contains a low power, high speed switching transistor (2N2222) with a coupling and biasing network. This stage is necessary for output waveform shaping, and it eliminates the frequency drift due to load variations. For this application the carrier frequency is hopped in a predetermined PR sequence between the frequencies of 1024 kHz and 1397 kHz.

The same schematic is used as a local oscillator in the receiver. For this purpose, C_1 and C_2 are changed to give new frequencies of 1690 kHz and 2063 kHz.

This provides the same hopping range of 1397 - 1024 = 373 kHz and 2063 - 1690 = 373 kHz, which provides a constant IF defined as

$$f_{LO} - f_c = 1690 - 1024 = 666 \text{ kHz}$$
$$= 2063 - 1397 = 666 \text{ kHz}$$

in the absence of data modulation.

Using the same type of VCO in the transmitter and receiver

helps the system have similar transient responses during the hopping intervals, decreases the possible mismatching of transmitter-receiver system, and simplifies the design.

Fig A-6 shows the schematic diagram of the delta modulator/demodulator. It is a single chip (MC 3418) continuously variable slope delta (CVSD) modulator/demodulator. The same chip can be used both as modulator or demodulator by connecting pin 15 to the resistor shown or to V_{cc} respectively. For this application, two chips are used: one as a modulator in the transmitter, and the other as a demodulator in the receiver. The resistor and capacitor values determine the clock rate of the system. Using the values shown in Fig A-6, voice input (300-3000 Hz) is digitized by a 25 kHz clock to give a 25 kilobit/sec output bit rate.

The mixer - IF amplifier section is shown in Fig A-7. The double balanced mixer (RELCOM-MI) provides a 50 dB carrier rejection. In this application the carrier frequency f_c = 1024 kHz and the intermediate frequency f_{IF} = 645 kHz are relatively close. Thus, carrier suppression at the output of the mixer is essential.

The IF amplifier has a relatively wide bandwidth ($\simeq$ 70 kHz). This is obtained by connecting a resistor (15 kΩ) in parallel with the output IF transformer. With perfect matching between the transmitter instantaneous frequency and the receiver local oscillator instantaneous frequency during the frequency hopping, the instantaneous IF varies between 620 kHz and 670 kHz.

This variation is caused by the two-level data. With a center frequency of 645 kHz, the IF amplifier bandwidth thus includes the main lobe of the signal spectrum. This bandwidth is obtained by adjusting the IF transformers. Finally, a single stage conventional IF amplifier provides the desired selectivity and voltage gain.

Fig A-8 shows the carrier demodulator schematic diagram. The input is the IF amplifier output. This IF signal is amplified and converted to a unipolar rectangular waveform by the discrete transistor limiter circuit. The voltage levels of this waveform are TTL compatible. Thus, the limiter output is directly connected to the monostable multivibrator (74121) input. The monostable multivibrator is adjusted to generate constant duration pulses (0.9 micro second) with the resistor and capacitor values shown. The averaging circuit consists of a second order RC lowpass filter. The values of the resistors and capacitors are chosen in such a way that the demodulated signal has negligibly small rise and fall times while the high frequency components (due to the pulse output of the monostable multivibrator) are filtered. The operation of this type of demodulator is discussed in the previous sections.

The demodulated signal is then amplified. A one-pole RC low-pass filter is used before the final stage of amplification. The final amplifier stage is used to interface the data, $d(t)$ with the delta demodulator.

In Fig A-9, a fourth-order Butterworth active low-pass filter is shown with the audio amplifier circuitry. The capacitor

and resistor values given determine the bandwidth of 3.1 kHz with a slope of 24 dB/octave. This filter produces the replica of the original message $v(t)$ at the delta demodulator output.

The audio amplifier is an IC type (LM 380). It provides the power (a few watts) needed to drive an 8 ohm speaker.
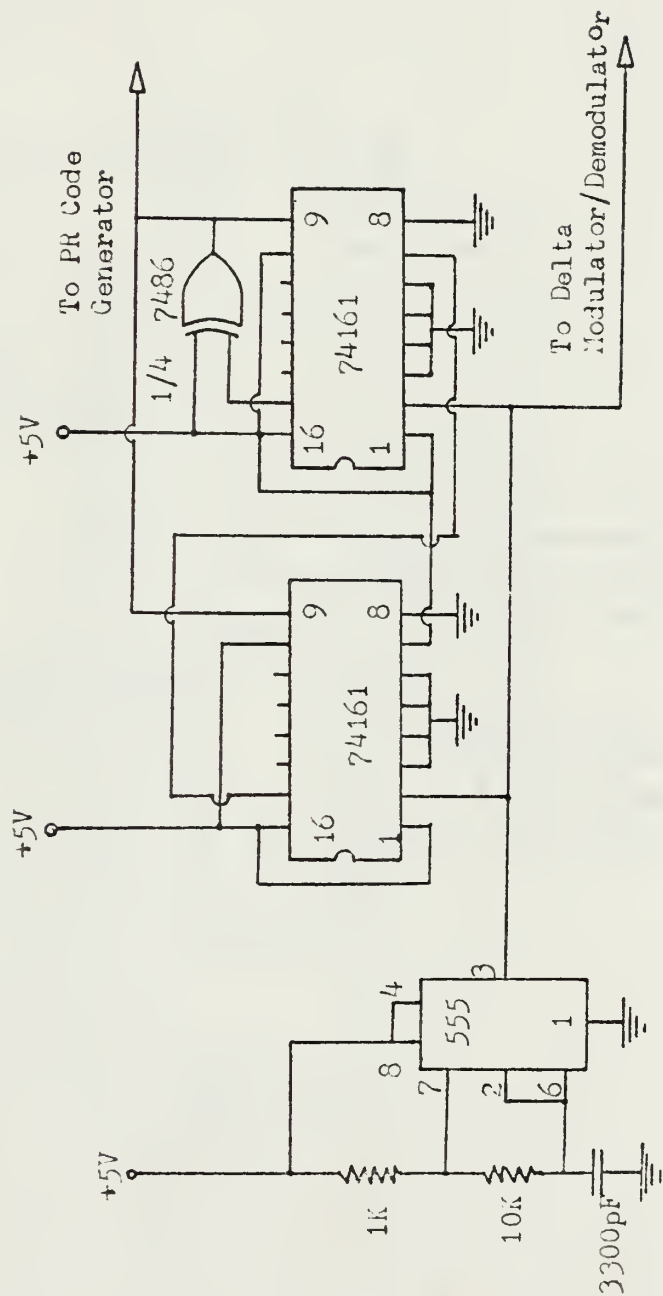
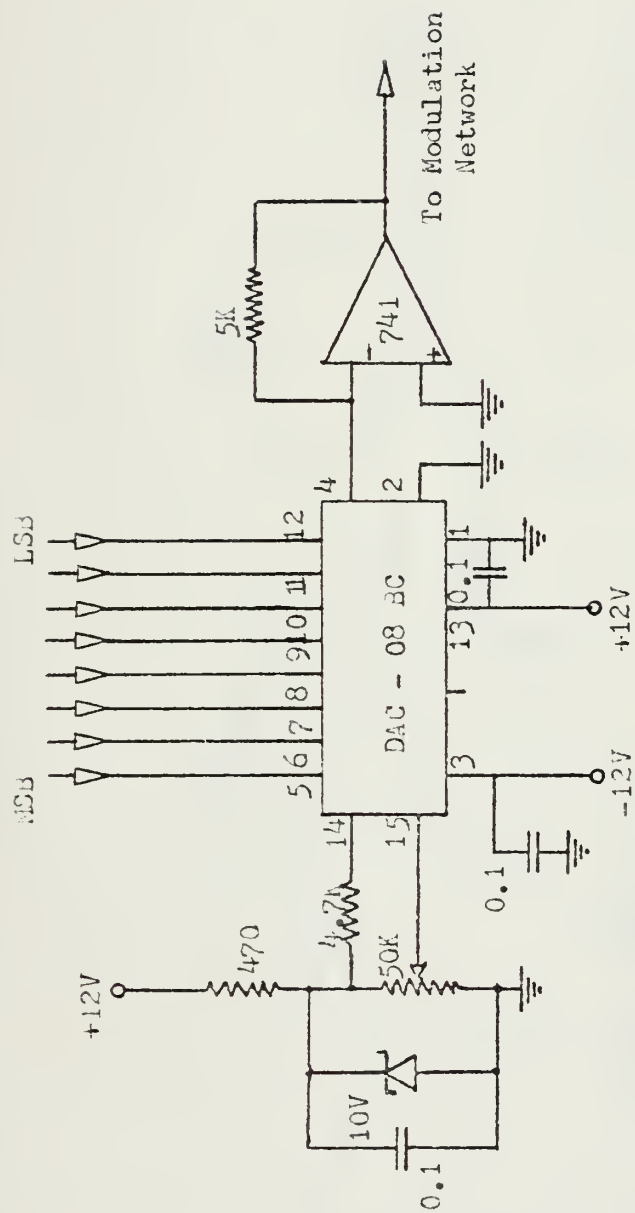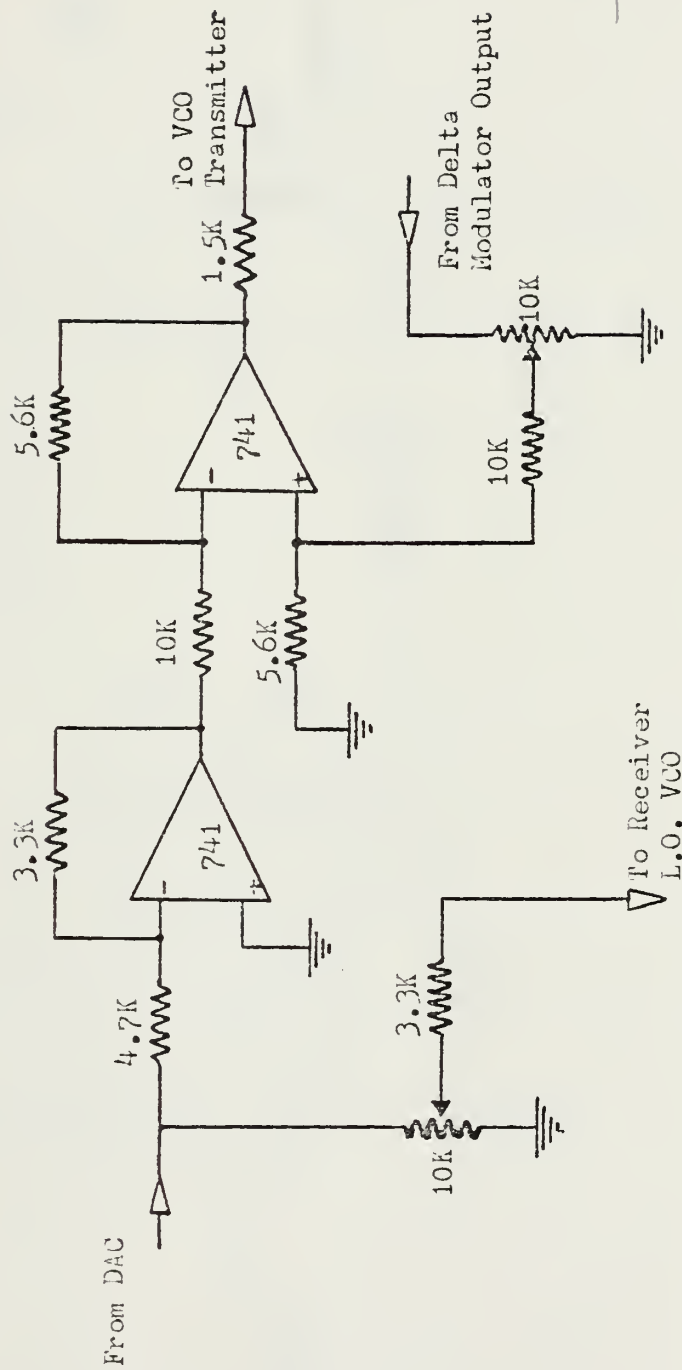FIG. A – 1.   CLOCK AND FREQUENCY DIVIDER

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From Frequency Divider

1/4 7486

1/4 7486

FIG. A – 2.   PR CODE GENERATOR WITH PROTECTION CIRCUIT

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FIG. A - 3 DAC

From DAC

To VCO
Transmitter

From Delta
Modulator Output

To Receiver
L.O. VCO

741

741

1.5K

5.6K

5.6K

10K

10K

10K

3.3K

3.3K

4.7K

10K

FIG. A - 4.   CARRIER   MODULATOR / HOPPING   CIRCUIT

FIG. A- 5   VOLTAGE CONTROLLED OSCILLATOR

$R_1, R_2 = 15K$

$C_1, C_2 = 270$ pF   L.O. Receiver   VCO

$C_1, C_2 = 470$ pF   Transmitter   VCO

FIG. A - 6   DELTA MODULATOR / DEMODULATOR

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FIG. A - 7 MIXER - IF AMPLIFIER

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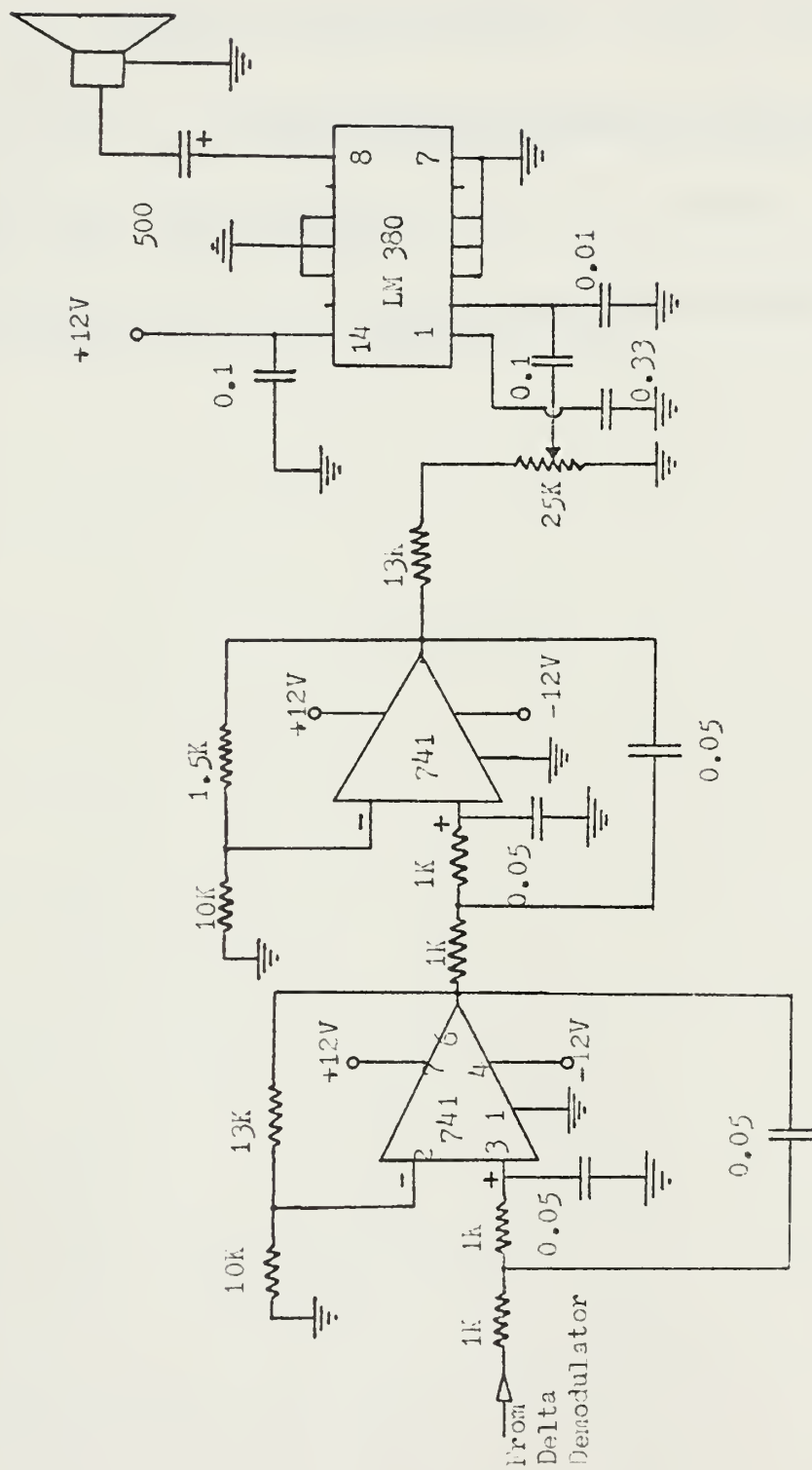FIG. A - 8. LIMITER - PCD - AMPLIFIER

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FIG. 4-9 LP FILTER – AUDIO AMPLIFIER

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